CLAIMS

1. A method of synchronizing a clock signal to a data signal, comprising the steps of:

(A) detecting a first edge of said data signal and a position of said first edge;

(B) determining if said position is within a zone;

(C) if said edge is not within said zone, adjusting said clock signal towards said position of said edge;

(D) detecting a second edge of said data signal and a position of said second edge;

(E) determining a in value indicating a position of said second edge;

(F) adding said first value to a second value, wherein said second value indicates a position of a third edge of said data signal; and

(G) adjusting said clock signal based on the result of step (F).

2. The method of claim 1, wherein step (E) further comprises:

comparing said third value to a predetermined value and adjust said clock signal only if said third value is greater than said predetermined value.

3. The method of claim 2, wherein step (B) further comprises:

determining if said third value is within a predetermined zone and adjusting said clock signal only if said third value is not within said zone.

4. The method of claim 3, wherein step (B) further comprises:

comparing said third value to said predetermined zone.

5. The method of claim 1, wherein step (E) further comprises selecting a number of clock phases based upon said third value.

6. The method of claim 1, wherein step (F) further comprises:

adjusting said third value in response to said second value when adding said first value and said second value would cause an overflow or underflow.

7. The method of claim 1, wherein step (E) further comprises:

incrementing or decrementing.

8. The method of claim 1, wherein step (F) further comprises:

storing said first value; and

storing said second value.

9. The method according to claim 1, wherein step (E) further comprises:

determining a high or low bandwidth.

10. The method according to claim 1, wherein step (E) further comprises:

determining a plurality of a phase offset magnitude.

11. The method according to claim 1, wherein step (E) further comprises:

determining a magnitude of said third value.

12. A method of synchronizing a clock signal to a data signal, comprising the steps of:

(A) upon power-up, performing said synchronization with a high bandwidth system; and

(B) after a predetermined amount of time, performing said synchronization with a low bandwidth system.

13. An apparatus for synchronization of a clock signal to a data signal, comprising:

a detector configured to synchronize with a high bandwidth system wherein said detection is configured after a predetermined amount of time preferring said synchronization with a low bandwidth system.

14. The apparatus of claim 13, wherein the detector comprises an accumulator that adds a first value to a second value

to produce a third value, wherein said second value represents a position of a second edge of said data signal.

15. The apparatus of claim 14, wherein the detector is further configured to compare said third value to a predetermined value and adjust said clock signal only if said third value is greater than said predetermined value.

16. The apparatus of claim 14, wherein the detector is further configured to determine if said first value is within a predetermined zone and to adjust said clock signal only if said value is not within said zone.

17. The apparatus of claim 14, wherein the detector further comprises a register configured to store said second value, a register configured to store said value, and an adder configured to add said value and said second value.

18. The apparatus of claim 13, wherein said detector further comprises:

a comparator configured to compare said third value to said predetermined value; and

a look ahead circuit configured to generate an enable signal in response to overflow or underflow condition.

19. The apparatus of claim 18, wherein said detector further comprises an increment/decrement logic circuit configured to adjust a third value in response to said second value and said enable signal.

20. The apparatus of claim 13, wherein said clock signal comprises a plurality of phases and said detector is configured to select one or said plurality of phases as system clock.